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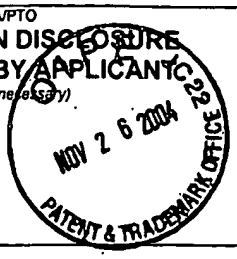

Complete if Known	
Application Number	09/943,134
Filing Date	August 30, 2001
First Named Inventor	Forbes, Leonard
Group Art Unit	2818
Examiner Name	Ho, Tu-Tu
Sheet 1 of 1	Attorney Docket No: 1303.020US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date if Appropriate
TH	US-5,474,947	12/12/1995	Chang, K. , et al.	12/27/1993
TH	US-6,009,011	12/28/1999	Yamauchi, Y.	12/24/1997
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

EXAMINER Tu-Tu Ho DATE CONSIDERED 03/31/2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Tu-Tu Ho
Serial No.:	09/943,134	Group Art Unit: 2818
Filed:	August 30, 2001	Docket: 1303.020US1
Title:	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Noted-
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Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/945507	August 30, 2001	1303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945395 6754108	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945498 6778441	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/028001	December 20, 2001	1303.035US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

Noted
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10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/789038	February 27, 2004	1303.024US2	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
10/783695	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/781035	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/929916	August 30, 2004	1303.035US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/788810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/931704	September 1, 2004	1303.014US2	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/929986	August 30, 2004	1303.045US2	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS

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10/931540	August 31, 2004	1303.020US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS

Respectfully submitted,

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Date 23 Nov '04 By

Timothy B. Clise
Reg. No. 40,957

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